87. (As Filed) The device of claim 66, wherein said second plurality of contact holes are formed by a dry etch process.

88. (Previously Once Amended) The device of claim 66, wherein said second plurality of contact holes are filled by a CVD process.

REMARKS

Claims 1-28, 30-39, 41-43, 45-70, 72-80 and 82-88 were pending in this application. Claims 12, 17, 32 and 41 have been amended, no claims have been either canceled or added. Hence, claims 1-28, 30-39, 41-43, 45-70, 72-80 and 82-88 remain pending. Reconsideration of the subject application as amended is respectfully requested.

In claims 12, 17, 32 and 41 Examiner has objected that it is not clear in these claims that "the first contact hole is of substantially equal depth to all the other holes in the first layer."

Claims 1-88 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Gutierrez, U. S. Patent No. 5,069,749 in view of Hashimoto et al., U. S. Patent No. 5,320,979.

FORMAL MATTERS

Claims 12, 17, 32 and 41 have been amended to overcome the objection based on impermissible recapture. Office Action at pgs. 2 and 6. Accordingly, Applicant respectfully requests withdrawal of the objection.

More specifically, amendments to claims 12, 17, 32 and 41 overcome the objection as "[a] broadened claim can be presented within two years from the grant of the original patent in a reissue application" and further, such broadened claims "avoid the effect of the recapture rule if the claims are broader in a way that does not attempt to reclaim what was surrendered earlier." MPEP §§ 1412.02 and 1412.03. This refers to reclaiming surrendered

scope, and is not necessarily limited to a surrendered limitation. Thus, because the claims at issue include a "narrowing limitation which modifies the claim in such a manner that the scope of the claim no longer results in a recapture of the surrendered subject matter, then there is no recapture" and they are permissible. MPEP § 1412.02.

Moreover, the claims as amended not only avoid the recapture rule, but each clarify that the first contact hole is of substantially equal depth to other holes in the first layer. Office Action at pg. 2. Specifically, claims 17, 32 and 41 are amended to include the following limitation: "wherein a thickness of the first insulating layer is substantially uniform". For this additional reason, the objection is overcome and withdrawal of the objection is respectfully requested.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103

Claims 1-88 are rejected under 35 U.S.C. 103 as being unpatentable over Gutierrez in view of Hashimoto et al. Office Action at pg. 2. These rejections are respectfully traversed in part and overcome in part.

Applicant claims an invention which, *inter alia*, provides a method for forming multi-layer interconnects in a way that each level of the interconnect is aligned with lower levels. More specifically, the conductive material formed in a via of a lower level is "overgrown appropriately to prevent misalignment with a second contact hole to be formed above the first contact hole." Applicant Patent at Fig. 2B; col. 3, lns. 40-43. Thus, the via is tapered to ensure alignment between interconnect layers. Furthermore, the conductive material is formed in the via by one single step.

Gutierrez teaches a method for forming a semiconductor-insulator layer with a planar surface. Specifically, the surface is made planar in an effort to avoid step coverage of succeeding layers. Gutierrez at col. 1, lns. 36-49; col. 4, lns. 42-44. The methods can be related to multi-level interconnects. Gutierrez at Fig. 8. However, Gutierrez does not disclose, teach, or even suggest a method for aligning different levels of a multi-layer interconnect. Indeed, Gutierrez does not even recognize the problem of misalignment.

The method of Gutierrez involves disposing a seed layer over a substrate. Gutierrez at Fig. 1; col. 3, lns. 23-33. Next, using lithographic techniques, a pattern, including a via exposing the seed material, is provided over the substrate. Gutierrez at Fig. 4; col. 3, lns. 34-50. Next, the method involves a "*first step*" of filling the via with Tungsten which continues until the seed layer is sacrificed. Gutierrez at Fig. 5; col. 3, ln. 57 - col. 4, ln. 20. Then, a "*next step*" is performed which finishes filling the via. Gutierrez at Fig. 6; col. 4, lns. 21-43. Thus, Gutierrez teaches a multi-step process for filling vias in a single layer. It should be recognized that the same two steps are required where the silicon substrate is the seed. See, e.g., Gutierrez at col. 5, lns. 11-24. Of no surprise, Gutierrez fails to disclose, teach or suggest a single step process for filling vias on a single layer.

Hashimoto teaches a method for forming a tapered, single layer via. The purpose of the taper is to increase the "burying rate (deposited film thickness in connection hole/deposited film thickness on a flat surface)". Hashimoto at col. 1, lns. 46-60. Furthermore, Hashimoto teaches that tapering the edges of the via provides for uniform wiring thickness when a conductive layer is deposited over a via which is 80% filled. Hashimoto at col. 3; lns. 12-18 and 24-29. Specifically, Hashimoto teaches that the vias are never completely filled, but rather only partially filled before an interconnect layer is deposited. Thus, the method of Hashimoto is incompatible with multi-level interconnects as claimed by Applicant.

Further, it should be noted that Hashimoto does not disclose, teach or suggest a method for aligning interconnect between layers. Indeed, similar to Gutierrez, Hashimoto fails to even recognize the problem of misalignment.

The method of Hashimoto comprises forming a highly vertical via using lithographic techniques. Then, similar to Gutierrez, a multi-step process of filling the via with a conductive material is performed. Hashimoto at Figs. 1C, 1E; col. 4, lns. 26-29. Accordingly, Hashimoto fails to disclose, teach or suggest a single step process for filling vias on a single layer.

In an interim step performed between the aforementioned filling steps, Hashimoto teaches a method for tapering an upper portion of the via. Hashimoto at Fig. 1D; col. 4, lns. 26-29. In fact, the tapering is partially controlled by the conductive material formed

in the via during the initial fill step. Hashimoto at Fig. 1D. This is in direct contradiction to filling the via in a single step as claimed by applicant.

Any combination of references cannot disclose, teach, or suggest what none of the references individually contain. Therefore, the combination of Hashimoto and Gutierrez does not disclose, teach or suggest a multi-level interconnect where the first level is tapered to promote alignment nor does the combination disclose, teach or suggest filling a first level of a multi-level interconnect using a single step process. Accordingly, Applicant respectfully requests withdrawal of the rejection and allowance of claims 1-28, 30-39, 41-43, 45-70, 72-80 and 82-88.

More specifically, it is asserted that "[o]ne of ordinary skill in the art would have been motivated use tapered openings to get better step coverage with tighter packing at the bottom of the opening." Office Action at pg. 4. However, assuming, arguendo, that such a teaching is provided by either Hashimoto, Gutierrez, or any combination thereof, it still does not in any way disclose, teach or suggest a tapered via to improve alignment. As clearly taught by Hashimoto, using a tapered opening to get better step coverage is critical where a via contacts a conductive layer. Hashimoto does not teach that it is even important at the interface between layers of a multi-layer interconnect. Indeed, Gutierrez reinforces the implicit teaching of Hashimoto that a taper at the interface between layers of a multi-layer interconnect is not important. Thus, at the absolute most, a combination of Gutierrez and Hashimoto may, perhaps motivate one skilled in the art to taper the top level of a multi-layer interconnect which is connected to a conductive layer. However, the combination of Hashimoto and Gutierrez does not disclose, teach, or suggest a taper in a lower level via as claimed by applicant.

In addition, the inability of the combination of Gutierrez and Hashimoto to render Applicant's claims obvious is, perhaps, most clear where the teachings of Hashimoto must first be subjected to a strained interpretation process before they can support any obviousness rejection. Specifically, it is asserted that Hashimoto "teach[es] that CVD tungsten *could* be grown above the holes, and then etched back leaving a landing pad for the next conductive deposit. . ." Office Action at pg. 4 *citing* Hashimoto at col. 6, lns. 42-45. First, the standard is not that such a thing "*could*" be so, it is that the combination discloses, teaches, or suggests it. See e.g. MPEP § 2143.01 *citing* In re Mills, 916 F.2d 680, 16 USPQ2d 1430 (Fed.

Cir. 1990). Second, and perhaps most important, Hashimoto does not disclose, teach or suggest what is asserted. More specifically, the cited portion of Hashimoto says:

> In addition, a selective growth method is used as a deposition method of the metal, but another method such as a combination of a normal CVD method and an etch-back may be used.

Hashimoto at col. 6, lns. 42-45. This cannot mean that the conductive material is grown beyond the via as this would potentially overflow and contact conductive material in adjacent vias causing shorts which would violate one of the stated purposes of Hashimoto (See *e.g.;* Hashimoto at col. 3, lns. 13-17).

The alternative interpretation of the cited portion of Hashimoto is even more fantastic. Assuming, arguendo, that it is possible to grow the conductive material beyond the via without the potential of shorts, it clearly would comprise multiple steps, including growth and etch back. Thus, the combination Gutierrez and Hashimoto would require multiple steps to fill a via at a single level. Such a configuration could not render a single step process, as claimed by Applicant, obvious.

As to the rejection of claims 5 and 10, it is asserted that Gutierrez teaches filling a via on a layer with a "single step" and/or in a "continuous step". This assertion is at war with Gutierrez itself. Indeed, Gutierrez discloses a "first step" followed by a "next step" which is clearly and explicitly two steps. Gutierrez at Figs. 5-6; col. 3, ln. 57 - col. 4, ln. 43. Any other interpretation cannot be supported by the cited art. Moreover, Hashimoto also clearly and explicitly discloses filling the via in a multi-step process. Thus, in light of the clear and explicit teachings of Gutierrez and Hashimoto, it would not have been obvious to one of ordinary skill in the art to fill the via in a single or step.

Further, a number of claims and/or limitations are rejected under an assertion that they are "well known" in the prior art. Applicant respectfully traverses and requests citation of specific references, rather than reliance on bald assertions. See e.g., MPEP § 2144.03.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

Douglas M. Hamilton
Reg. No. P-47,629

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San francisco, CA 94111-3834

Tel: (303) 571-4000
Fax: (303) 571-4321

DMH:sbm
DE 7030645 v1

OIPE JC13
FEB 1 3 2001
PATENT & TRADEMARK OFFICE

APPENDIX A

U. S. Patent Application No. 09/434,736, filed November 2, 1999
Claims as filed in Amendment responding to Office Action mailed November 9, 2000
Amendment Filed with USPTO February 9, 2001

A marked up copy of the claims showing the most recent amendments is provided below in accordance with 37 CFR § 1.121(c). All pending claims are set forth below for convenient reference.

1. (As filed) A method for filling contact holes with metal by two-step deposition of metal layers, said method comprising the steps of:

providing a silicon substrate;

forming a field oxide layer and a junction layer and gate electrode on said silicon substrate;

forming a first insulating layer on exposed portions of the field oxide layer, the junction layer, and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively the first plurality of contact holes having a tapered upper portion;

filling a first metal layer into the first plurality of contact holes, entirely, the first metal layer being grown over and extending slightly beyond said first plurality of contact hoes;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively and

filling a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern respectively.

2. (As Filed) A method according to claim 1, wherein the first metal layer and subsequently the second metal layer are formed by chemical vapor deposition method.

3. (Previously Once Amended) A method according to claim 1, wherein the filling a second metal layer fills the second plurality of contact holes to a substantially equal depth.

4. (As Filed) A method according to claim 1, wherein the first and second metal layers are selective tungsten layers, respectively, and the first and second plurality of contact holes are filled with the first and second metal layers of the selected tungsten layers, respectively.

5. (As Filed) A method for filling contact holes with metal by a two-step deposition of metal layers, said method comprising the steps of:

providing a silicon substrate;

forming a field oxide layer and a junction layer and gate electrode on said silicon substrate;

forming a first insulating layer on exposed portions of the field oxide layer, the junction layer, and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively the first plurality of contact holes having a tapered upper portion;

filling a first metal layer into entire first plurality of contact holes by one single step, the first metal layer being grown over and extending slightly beyond said first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively and

filling a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern respectively.

6. (As Filed) A method of forming a substrate with contact holes, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively, the first plurality of contact holes having a tapered upper portion;

forming a first conductive material layer into the first plurality of contact holes, entirely, the first conductive material layer being grown over and extending slightly beyond said first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern, respectively; and

forming a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern, respectively.

7. (Previously Once Amended) A method according to claim 6, wherein the first conductive material layer and subsequently the second conductive material layer are formed by a chemical vapor deposition process.

8. (Previously Once Amended) A method according to claim 6, wherein the forming a second conductive material layer fills the second plurality of contact holes to a substantially equal depth.

9. (Previously Once Amended) A method according to claim 6, wherein the first and second conductive material layers comprise first and second tungsten layers, respectively, and the first and second plurality of contact holes are filled with the first and second tungsten layers, respectively.

10. (As Filed) A method of forming a substrate with contact holes, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively, the first plurality of contact holes having a tapered upper portion;

forming a first conductive material layer into entire first plurality of contact holes in a continuous step, the first conductive material layer being grown over and extending slightly beyond said first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern, respectively; and

forming a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern, respectively.

11. (As Filed) A method according to claim 10, wherein said steps of forming said first and said second conductive material layers comprise filling said first and said second plurality of contact holes, respectively.

12. (Twice Amended Herein) A method of forming a substrate with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer and a junction layer on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the junction layer;

forming a first contact hole of substantially equal depth to other **[another]** contact holes **[hole]** in the first insulating layer by removing a portion of the first insulating layer to expose said junction layer, the first contact hole having a tapered upper portion;

forming a first conductive material layer into the first contact hole, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first contact hole;

forming a second contact hole by removing portions of said second insulating layer to expose the first conductive material layer; and

forming a second conductive material layer into said second contact hole to contact the first conductive material layer.

13. (As Filed) A method as in claim 12, further comprising:

forming a third contact hole by removing portions of the second insulating layer to expose the conductive layer pattern; and

forming the second conductive material layer into the third contact hole to contact the conductive layer pattern.

14. (As Filed) A method as in claim 12, wherein said first and said second conductive material layers comprise a metal.

15. (Previously Once Amended) A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a silicon substrate;

forming an oxide layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said gate electrode, the first plurality of contact holes having a tapered upper portion;

filling a first conductive material layer into the first plurality of contact holes, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern; and

filling a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern.

16. (As Filed) A method as in claim 15, wherein said first and second conductive material layers comprise first and second metal layers.

17. (Once Amended Herein) A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive material layers, said method comprising:

providing a substrate;

forming an oxide layer and a first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the first conductive layer pattern, wherein a thickness of the first insulating layer is substantially uniform;

forming a first contact hole by removing a portion of the first insulating layer to expose said first conductive layer pattern, the first contact hole having a tapered upper portion;

forming a first conductive material layer into the first contact hole, filling said first contact hole entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first conductive material layer;

forming second and third contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the second conductive layer pattern, respectively; and

forming a second conductive material layer into said second and third contact holes to contact the first conductive material layer and the second conductive layer pattern, respectively.

18. (As Filed) A method as in claim 17, wherein said first conductive layer pattern comprises a gate electrode.

19. (As Filed) A method as in claim 17, wherein said first and second conductive material layers comprise first and second metal layers.

20. (As Filed) A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the first conductive layer pattern;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said first conductive layer pattern, respectively, the first plurality of contact holes having a tapered upper portion;

filling a first conductive material layer into the first plurality of contact holes, entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the second conductive layer pattern, respectively; and

filling a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the second conductive layer pattern, respectively.

21. (As Filed) A method as in claim 20, wherein said first and second conductive material layers comprise first and second metal layers.

22. (As Filed) A method as in claim 20, wherein said first conductive layer pattern comprises a gate electrode.

23. (As Filed) A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer, and first and second regions on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and said first and said second regions;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said first and second regions, the first plurality of contact holes having a tapered upper portion;

forming a first conductive material layer into, and filling entirely, the first plurality of contact holes;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first conductive material layer;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern; and

forming a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern.

24. (As Filed) A method as in claim 23, wherein said first region comprises a junction layer.

25. (As Filed) A method as in claim 23, wherein said second region comprises a gate electrode.

26. (As Filed) A method as in claim 23, wherein said first and second conductive material layers comprise first and second metal layers.

27. (Previously Once Amended) A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive layers, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively, wherein said first plurality of contact holes have an upper portion width and a lower portion width, said upper portion width greater than said lower portion width;

forming a first conductive material layer into the first plurality of contact holes, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first conductive material layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the conductive layer pattern; and

forming a second conductive material layer into said second plurality of contact holes to contact the first conductive material layer and the conductive layer pattern.

28. (As Filed) A method as in claim 27, wherein said first and second conductive material layers comprise first and second metal layers.

30. (As Filed) A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer and a junction layer on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the junction layer;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer, the first plurality of contact holes having a tapered upper portion;

forming a first metal layer into the first plurality of contact holes, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

forming a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

31. (As Filed) A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said gate electrode, the first plurality of contact holes having a tapered upper portion;

filling a first metal layer into the first plurality of contact holes, entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

filling a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

32. (Once Amended Herein) A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer and a first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the first conductive layer pattern, wherein a thickness of the first insulating layer is substantially uniform;

forming a first contact hole by removing a portion of the first insulating layer to expose said first conductive layer pattern, the first contact hole having a tapered upper portion;

forming a first metal layer into the first plurality of contact hole, entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first contact hole;

forming second and third contact holes of substantially equal depth by removing portions of said second insulating layer to expose the first metal layer and the second conductive layer pattern, respectively; and

forming a second metal layer into said second and third contact holes to contact the first metal layer and the second conductive layer pattern, respectively.

33. (As Filed) A method as in claim 32, wherein said first conductive layer pattern comprises a gate electrode.

34. (As Filed) A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer and a junction layer and first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the first conductive layer pattern;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said first conductive layer pattern, respectively, the first plurality of contact holes having a tapered upper portion;

forming a first metal layer into the first plurality of contact holes, entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the second conductive layer pattern, respectively; and

forming a second metal layer into said second plurality of contact holes to contact the first metal layer and the second conductive layer pattern, respectively.

35. (As Filed) A method as in claim 34, wherein said first conductive layer pattern comprises a gate electrode.

36. (As Filed) A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer, and first and second regions on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the first region and the second region;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said first and said second region, respectively, the first plurality of contact holes having a tapered upper portion;

forming a first metal layer into the first plurality of contact holes, to fill said first plurality of contact holes entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

forming a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

37. (As Filed) A method as in claim 36, wherein said first region comprises a junction layer.

38. (As Filed) A method as in claim 36, wherein said second region comprises a gate electrode.

39. (Previously Once Amended) A method of forming a semiconductor with contact holes filled by multi-step deposition of metal layers, said method comprising:

providing a substrate;

forming an oxide layer, a junction layer and a gate electrode on said substrate;

forming a first insulating layer on exposed portions of the oxide layer, the junction layer, and the gate electrode;

forming first plurality of contact holes of substantially equal depth by removing portions of the first insulating layer to expose said junction layer and said gate electrode, respectively, wherein said first plurality of contact holes have a tapered upper portion;

forming a first metal layer into the first plurality of contact holes, to fill said first plurality of contact holes entirely;

forming a conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the conductive layer pattern, the first insulating layer, and the first plurality of contact holes;

forming second plurality of contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first metal layer and the conductive layer pattern, respectively; and

forming a second metal layer into said second plurality of contact holes to contact the first metal layer and the conductive layer pattern, respectively.

41. (Twice Amended Herein) A method of forming a semiconductor with contact holes filled by multi-step deposition of conductive material layers, said method comprising:

providing a substrate;

forming an oxide layer and a first conductive layer pattern on said substrate;

forming a first insulating layer on exposed portions of the oxide layer and the first conductive layer pattern, wherein a thickness of the first insulating layer is substantially uniform;

forming a first contact hole by removing portions of the first insulating layer to expose said first conductive layer pattern, wherein said first contact hole has an upper portion width and a lower portion width, said upper portion width greater than said lower portion width;

forming a first conductive material layer into the first contact hole, entirely;

forming a second conductive layer pattern on the first insulating layer spaced from said first metal layer;

forming a second insulating layer on exposed portions of the second conductive layer pattern, the first insulating layer, and the first contact hole;

forming second and third contact holes of substantially equal depth by removing portions of said second insulating layer to expose both the first conductive material layer and the second conductive layer pattern, respectively; and

forming a second conductive material layer into said second and said third contact holes to contact the first conductive material layer and the second conductive layer pattern, respectively.

42. (As Filed) The method of claim 41, wherein said first conductive material layer comprises a metal.

43. (As Filed) The method of claim 42, wherein said metal comprises tungsten.

45. (As Filed) The method of claim 41, wherein said first conductive layer pattern comprises a gate electrode.

46. (As Filed) The method of claim 41, wherein said first conductive layer pattern comprises a gate electrode overlying a gate oxide.

47. (Previously Once Amended) The method of claim 41, wherein said forming an oxide layer and a first conductive layer pattern further comprises forming a junction layer.

48. (As Filed) The method of claim 41, wherein said junction layer comprises a N+ junction.

49. (As Filed) The method of claim 41, wherein said junction layer comprises a P+ junction.

50. (As Filed) The method of claim 41, wherein said first conductive layer pattern comprises polysilicon.

51. (As Filed) The method of claim 41, wherein said first insulating layer comprises a first oxide layer.

52. (As Filed) The method of claim 41, wherein said step of forming said first contact hole comprises a photoresist process.

53. (As Filed) The method of claim 41, wherein said step of forming said first contact hole comprises a wet etch process.

54. (As Filed) The method of claim 41, wherein said step of forming said first contact hole comprises a dry etch process.

55. (As Filed) The method of claim 47, wherein said step of forming said first contact hole further exposes said junction layer.

56. (As Filed) The method of claim 41, wherein said first contact hole has a tapered upper portion.

57. (As Filed) The method of claim 41, wherein said step of forming said first conductive material layer comprises a CVD process.

58. (As Filed) The method of claim 41, wherein said second conductive layer pattern comprises polysilicon.

59. (As Filed) The method of claim 41, wherein said second insulating layer comprises a second oxide layer.

60. (As Filed) The method of claim 41, wherein said step of forming said second and said third contact holes comprises a photoresist process.

61. (As Filed) The method of claim 41, wherein said step of forming said second and said third contact holes comprises a wet etch process.

62. (As Filed) The method of claim 41, wherein said step of forming said second and said third contact holes comprises a dry etch process.

63. (As Filed) The method of claim 41, wherein said step of forming said second conductive material layer comprises a CVD process.

64. (As Filed) A semiconductor device comprising:

a semiconductor substrate having an oxide layer, a junction layer and a gate electrode;

a first insulating layer overlying portions of said oxide layer, said junction layer and said gate electrode, said first insulating layer having a first plurality of contact holes of substantially equal depth over said junction layer and said gate electrode, said first plurality of contact holes having a tapered upper portion;

a first metal layer filling said first plurality of contact holes so that said first metal layer is in contact with said junction layer and said gate electrode;

a conductive layer pattern on said first insulating layer spaced apart from said first metal layer;

a second insulating layer overlying portions of said conductive layer pattern, said first insulating layer and said first plurality of contact holes, said second insulating layer having a

second plurality of contact holes of substantially equal depth over said first metal layer and said conductive layer pattern; and

a second metal layer filling said second plurality of contact holes, said second metal layer in contact with said first metal layer and said conductive layer pattern.

65. (As Filed) A semiconductor device comprising:

a semiconductor substrate having an oxide layer, a junction layer and a gate electrode;

a first insulating layer overlying portions of said oxide layer, said junction layer and said gate electrode, said first insulating layer having a first plurality of contact holes of substantially equal depth over said junction layer and said gate electrode, said first plurality of contact holes having a tapered upper portion;

a first conductive material layer filling said first plurality of contact holes so that said first conductive material layer is in contact with said junction layer and said gate electrode;

a conductive layer pattern on said first insulating layer spaced apart from said first conductive material layer;

a second insulating layer overlying portions of said conductive layer pattern, said first insulating layer and said first plurality of contact holes, said second insulating layer having a second plurality of contact holes of substantially equal depth over said first conductive material layer and said conductive layer pattern; and

a second conductive material layer filling said second plurality of contact holes, said second conductive material layer in contact with said first conductive material layer and said conductive layer pattern.

66. (Previously Once Amended) A semiconductor device comprising:

a semiconductor substrate having an oxide layer and a first conductive layer pattern;

a first insulating layer overlying portions of said oxide layer and said first conductive layer pattern, said first insulating layer having a first plurality of contact holes of substantially equal depth over said first conductive layer pattern, wherein said first plurality of contact holes have a tapered upper portion;

a first conductive material layer filling said first plurality of contact holes so that said first conductive material layer is in contact with said first conductive layer pattern;

a second conductive layer pattern on said first insulating layer spaced apart from said first conductive material layer;

a second insulating layer overlying portions of said second conductive layer pattern, said first insulating layer and said first plurality of contact holes, said second insulating layer having a second plurality of contact holes of substantially equal depth over said first conductive material layer and said second conductive layer pattern; and

a second conductive material layer filling said second plurality of contact holes, said second conductive material layer in contact with said first conductive material layer and said second conductive layer pattern.

67. (As Filed) The device of claim 66, wherein said conductive material layers comprise a metal.

68. (As Filed) The device of claim 67, wherein said metal comprises tungsten.

69. (As Filed) The device of claim 66, wherein said first conductive layer pattern comprises a gate electrode.

70. (As Filed) The device of claim 66, wherein said first conductive layer pattern comprises a gate electrode overlying a gate oxide.

72. (As Filed) The device of claim 66, further comprising a junction layer on said substrate.

73. (As Filed) The device of claim 72, wherein said junction layer comprises a N+ junction layer.

74. (As Filed) The device of claim 72, wherein said junction layer comprises a P+ junction layer.

75. (As Filed) The device of claim 66, wherein said first conductive layer pattern comprises polysilicon.

76. (As Filed) The device of claim 66, wherein said first insulating layer comprises a first oxide layer.

77. (As Filed) The device of claim 66, wherein said first plurality of contact holes are formed by a photoresist process.

78. (As Filed) The device of claim 66, wherein said first plurality of contact holes are formed by a wet etch process.

79. (As Filed) The device of claim 66, wherein said first plurality of contact holes are formed by a dry etch process.

80. (As Filed) The device of claim 72, wherein said first plurality of contact holes expose said junction layer.

82. (Previously Once Amended) The device of claim 66, wherein said first plurality of contact holes are filled by a CVD process.

83. (As Filed) The device of claim 66, wherein said second conductive layer pattern comprises polysilicon.

84. (As Filed) The device of claim 66, wherein said second insulating layer comprises a second oxide layer.

85. (As Filed) The device of claim 66, wherein said second plurality of contact holes are formed by a photoresist process.

86. (As Filed) The device of claim 66, wherein said second plurality of contact holes are formed by a wet etch process.

87. (As Filed) The device of claim 66, wherein said second plurality of contact holes are formed by a dry etch process.

88. (Previously Once Amended) The device of claim 66, wherein said second plurality of contact holes are filled by a CVD process.

DE 7030759 v1